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# Evaluation of Bidirectional Silicon Carbide Solid-State Circuit Breaker v3.2

**by D. Urciuoli**

**ARL-MR-0845** **July 2013**

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# Evaluation of Bidirectional Silicon Carbide Solid-State Circuit Breaker v3.2


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**Sensors and Electron Devices Directorate, ARL**

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**14. ABSTRACT**
Although solid-state switches can be actuated several orders of magnitude faster than electromechanical ones, most solid-state circuit breakers require some form of sensing, filtering, triggering, latching, and reset capability for control. These functions can contribute to undesirable delays that limit performance. Modifications were made to the design of a small-scale 600-V, 5-A silicon carbide (SiC) junction field-effect transistor (JFET) based bidirectional solid-state circuit breaker (BDSSCB) to reduce self-trigging and reset response times, and increase rated current to 10 A. Additional current rating increases are possible, while maintaining the small-scale BDSSCB footprint area of 32.2 $cm^2$ (5.0 $in^2$), using custom power stage designs. Experimental results are presented for both BDSSCBs evaluated in a pulsed current test circuit.

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## 1. Introduction

The U.S. Army Research Laboratory (ARL) completed the fabrication and evaluation of its most recent small-scale bidirectional solid-state circuit breaker (BDSSCB) design. This new implementation, designated BDSSCB v3.2, is another technical readiness level 5 (TRL5) prototype based on a normally on silicon carbide (SiC) junction field-effect transistor (JFET) power stage, and has the same overall size as the previous BDSSCB v3.1 design (*1*). The BDSSCB v3.1 and v3.2 topology is shown in figure 1. Through modifications to control hardware that was limiting power stage response times, BDSSCB v3.2 provides faster self-trip times and a faster reset time than v3.1. These upgrades provide improved fault protection and increase the modulation capability of the BDSSCB to support additional capabilities such as pre-charge and soft start. BDSSCB v3.2 also uses lower resistance JFETs, resulting in a higher current rating than the previous design.

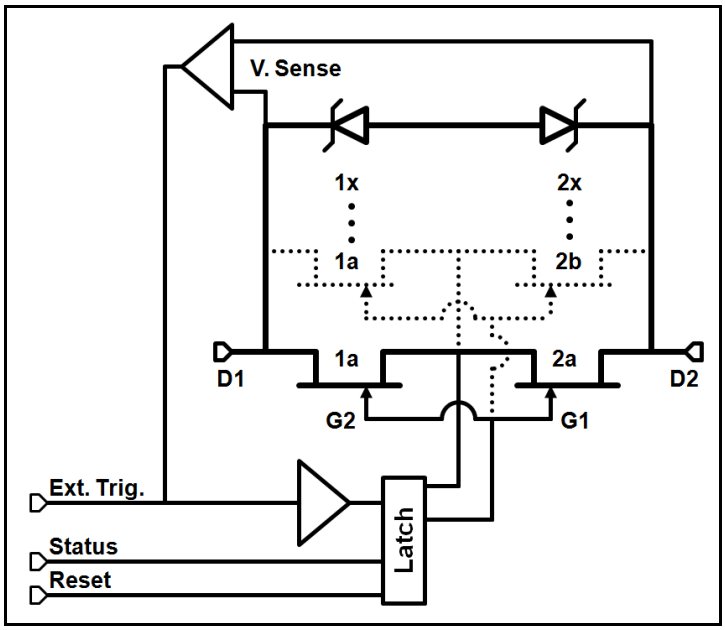



Figure 1. BDSSCB v3.1 and v3.2 topology block diagram.

## 2. BDSSCB v3.2 Prototype

A controller design revision was needed to improve the response times of BDSSCB v3.1. The v3.1 trigger and latch design used discrete components to trip at BDSSCB conduction voltage drops as low as 0.8 V to enable low power dissipation. Unfortunately, the design also resulted in long response times. Operating specifications for BDSSCB v3.1 are shown in the datasheet in the

appendix. Although the voltage blocking state of BDSSCB v3.1 was maintained during the 6.5- to 7.5-ms reset pulse to prevent an unprotected conduction state, the reset duration was a functional limitation. More importantly, the latch reset function also limited further reduction of the self trigger times of the v3.1 design. A design trade was made for an increase in the minimum conduction voltage drop at the BDSSCB trip point to reduce the trigger and reset times.

The controller and power stage were modified for BDSSCB v3.2, while preserving the overall benefits of the v3.1 design, such as adjustable over-current trip point, status output, and 800-V bidirectional blocking. The BDSSCB v3.2 prototype is shown in figure 2 and has the same 6.2-cm by 5.2-cm (2.44-in by 2.05-in) footprint and 2.8-cm (1.1-in) total height as the v3.1 design. The two circuit breaker terminals extend beyond the BDSSCB footprint on the right of figure 2. A single control connector is used for supply power, status feedback, external trigger, and reset signals. In addition to the trigger and latch, the isolated DC-DC converter was modified to improve stability. Finally, higher current rated SJDP120R045 SiC JFETs were used to increase the nominal DC trip current from 5 A to 10 A.

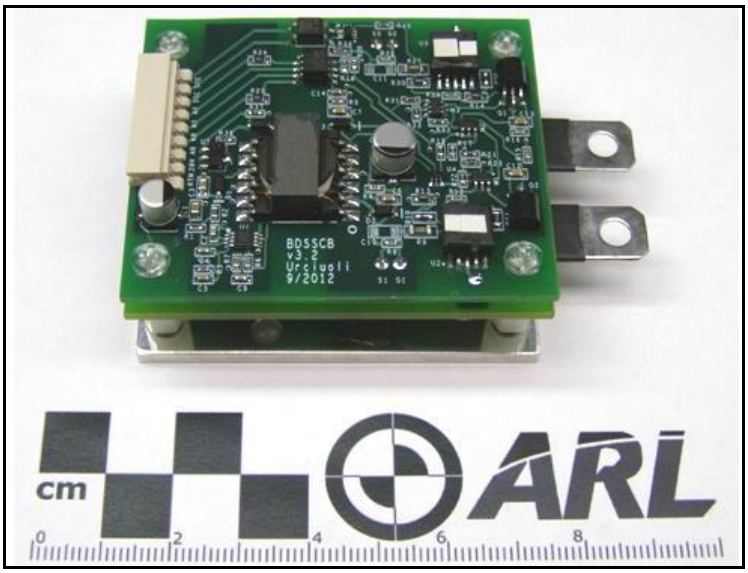



Figure 2. BDSSCB v3.2 prototype 6.2-cm by 5.2-cm footprint and 2.8-cm total height.

## 3. BDSSCB v3.2 Self Triggered Response

The range of pulse widths required to reset the latch was significantly reduced to 50 to 200 µs. Self trigger delay times were reduced by more than a factor of three and are shown in the BDSSCB v3.2 datasheet in the appendix. The self trigger delay time is reported as the total rise time of a current pulse conducted by the BDSSCB from an 80-µF capacitor bank, through a series 16-µH inductor and 16.7-Ω resistive load, to the start of the BDSSCB turn-off transition. The BDSSCB pulse current test circuit is shown in figure 3 (*1*). The DC supply charges the

capacitor through a high resistance. Then the insulated gate bipolar transistor (IGBT) is turned on to supply a pulse current to the BDSSCB, which then turns off by either a self trigger or an external trigger.

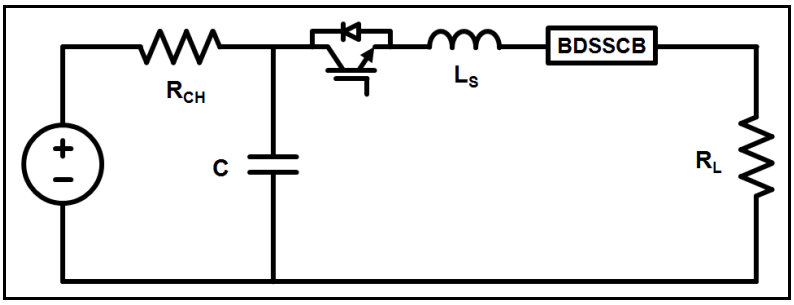
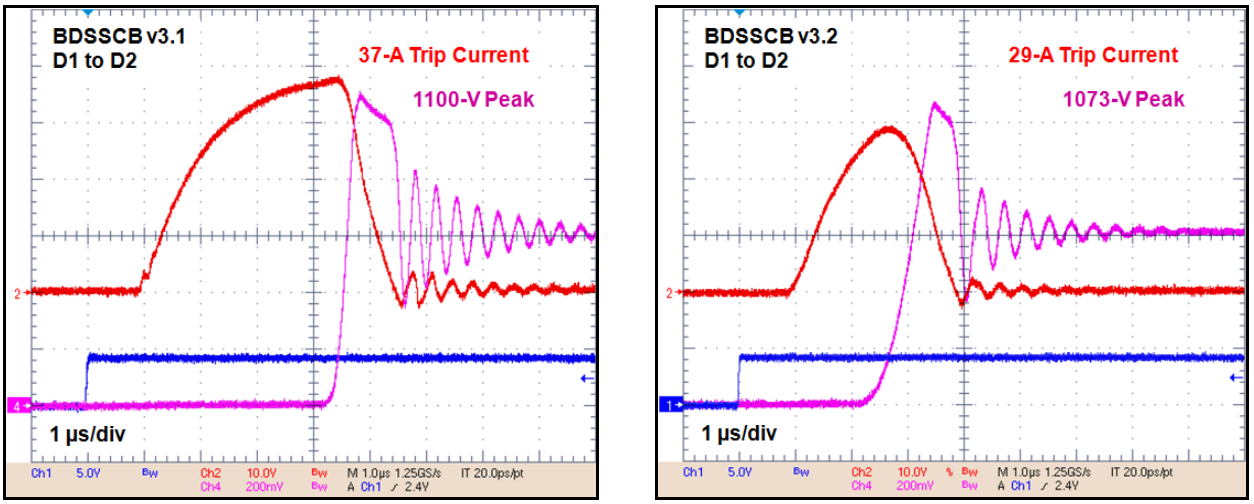



Figure 3. Pulse current test circuit for the BDSSCB.

The 16-µH inductor represents a series line inductance of a system having several feet of cabling and/or a loop area between the source and the load. Because this BDSSCB design is intended to be operated in a system as a floating high-side switch, it does not rely on additional freewheeling connections to the current return path between the load and the source. Thus, the 16-µH inductor in the test circuit provides the representative voltage stress across the BDSSCB, which is clamped by the transient voltage suppression diodes during the trip (turn-off) condition. However, the inductor also limits the rise time of the BDSSCB current pulse, thereby effectively increasing the self trigger time as measured from the test circuit. Figures 4a and b show the BDSSCB pulse current and terminal voltage waveforms for self triggering of the v3.1 and v3.2 designs, respectively, for a nominal 600-V source. The waveforms of figure 4b show a lower peak current and a lower peak voltage as a result of the faster v3.2 self triggering time. A supply voltage that is higher than the nominal voltage is used to drive each current pulse to overcome the resistance of circuit components and connections. For example, in figure 4a, the 37-A peak current slightly exceeds the expected peak current of 35.9 A for a 600-V supply and a 16.7-Ω load. Unlike the peak current in figure 4a, which is at approximately the maximum value for the test circuit, the peak current of figure 4b, has been limited by the BDSSCB v3.2 at a greater di/dt and has less dependence on the circuit load resistance.




a b

Figure 4. (a) BDSSCB v3.1 self triggering, D1 to D2, 600-V nominal, 37-A turn-off, 3.6-µs rise-time current pulse (left) and (b) BDSSCB v3.2 self triggering, D1 to D2, 600-V nominal, 29-A turn-off, 1.8-µs rise-time current pulse (right), (Ch1: IGBT turn-on signal, Ch2: BDSSCB pulse current, Ch4: BDSSCB voltage drop).

The self triggered response of BDSSCB v3.2 is markedly better than that of v3.1 when considering the BDSSCB steady state (DC) turn-off currents. The lower current rated SJDP120R085 SiC JFETs and the v3.1 controller design resulted in a 4.8-A DC turn-off current rating at a BDSSCB drain-to-drain voltage drop of 1.1 V, as shown on the v3.1 datasheet. Therefore, v3.1 self triggers at 7.7 times its DC turn-off current rating, 3.6 µs after the start of the current pulse shown in figure 4a. By contrast, the higher current rated SJDP120R045 SiC JFETs with the BDSSCB v3.2 control circuit modifications result in a 9.6-A DC turn-off current rating at a drain-to-drain voltage drop of 1.4 V. So, v3.2 self triggers at 3.0 times its DC turn-off current rating, 1.8 µs after the start of the current pulse shown in figure 4b. Although the v3.1 voltage drop at its trigger point was adjusted up to 1.1 V, the minimum BDSSCB self trigger voltage drops for the v3.1 and v3.2 designs are 0.8 and 1.4 V, respectively. These voltages represent the aforementioned tradeoff between BDSSCB response time and minimum conduction voltage drop at the trip point for the v3.x controller design. The 0.8- and 1.4-V values result in conduction losses of 0.13% and 0.23% for the v3.1 and v3.2 designs, respectively, when operated on a 600-V bus.

The self trigger delay times (start of current pulse to peak current) of BDSSCB v3.2 were evaluated in the test circuit of figure 3 over a range of nominal source voltages from 250 to 600 V. The minimum trigger point voltage drop of 1.4 V was used in the evaluation. Current pulse rise times were proportional to the source voltage used at each test point, resulting from the test circuit inductor. The BDSSCB was operated under the same test conditions with current flow in both directions (D1 to D2 and D2 to D1), and the current pulse durations and peak trip currents were averaged for each test condition. Figure 5 shows the average self trigger delay time versus the peak trip current over the range of source voltages. Although the pulse rise

time was governed by the source voltage and the circuit inductor, and was therefore not constant over the test range, the self trip response times exhibit a trend similar to that of a fuse. Another factor contributing to the trend is the delay introduced by a filter designed to prevent false triggering from typical circuit transients.

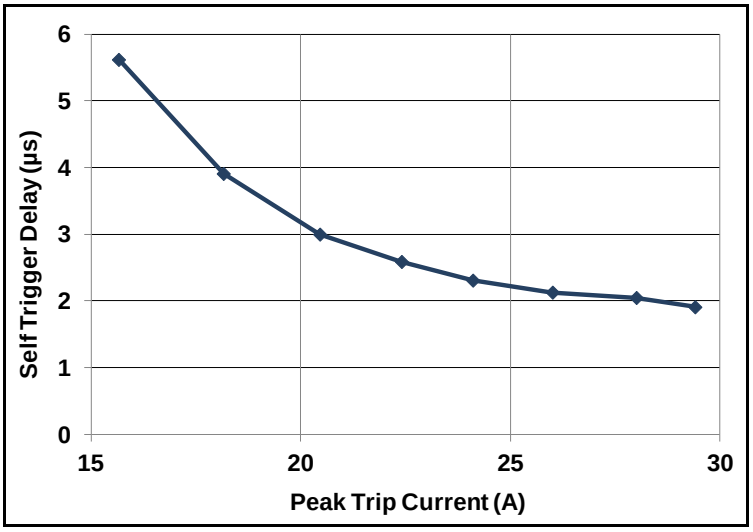
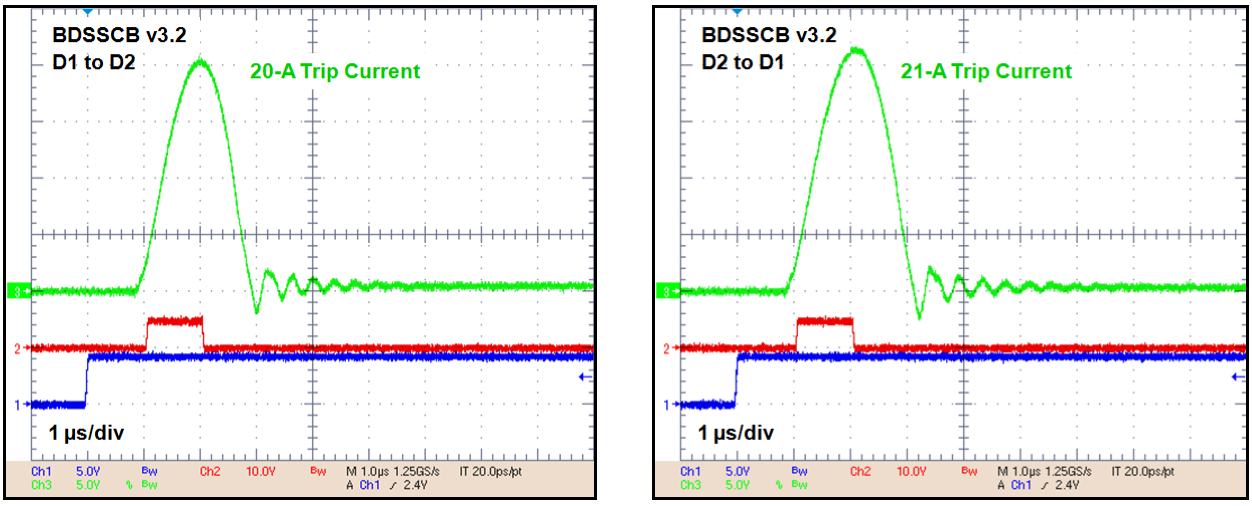



Figure 5. Average self trigger delay vs. peak trip current over 250- to 600-V source range

## 4. BDSSCB v3.2 Externally Triggered Response

The isolated external trigger input allows the BDSSCB to be tripped by an external control signal. The external trigger delay time, as measured from the start of the external trigger pulse to the peak BDSSCB current at the start of the turn-off transition was 1 µs. This delay time was observed for BDSSCB v3.2 conduction in both directions (D1 to D2 and D2 to D1) with a nominal 600-V test circuit source. Figures 6a and b show the BDSSCB pulse currents for external triggering of the v3.2 design in both conduction directions.




a b

Figure 6. (a) BDSSCB v3.2 external triggering, D1 to D2, 600-V nominal, 20-A turn-off, 1-µs rise-time current pulse (left) and (b) BDSSCB v3.2 external triggering, D2 to D1, 600-V nominal, 21-A turn-off, 1-µs rise-time current pulse (right), (Ch1: IGBT turn-on signal, Ch2: external trigger pulse, Ch3: BDSSCB pulse current).

## 5. Conclusion

The design of the small-scale BDSSCB v3.1 was modified to enable faster self triggering and faster reset times. The new BDSSCB v3.2 prototype was built with a larger 10-A power stage and improved power supply stability in the same 6.2-cm by 5.2-cm (2.44-in by 2.05-in) footprint and 2.8-cm (1.1-in) height. Evaluations of the v3.2 design in a pulsed current test circuit exhibited reductions in self trigger delay times (start of current pulse to peak current) by more than a factor of three, along with a 97% to 99% reduction in reset time. However, the minimum BDSSCB voltage drop at the self trigger point increased from 0.8 to 1.4 V, resulting in a 0.1% increase in conduction loss during operation on a 600-V bus. External trigger delay time from the start of an external trigger pulse to the peak current at BDSSCB turn-off was 1 µs. Overall, BDSSCB v3.2 provides improved performance over previous designs and can accept higher current rated power stages while maintaining the same footprint size.

The SiC JFET components produced by SemiSouth Laboratories, Inc., that were used in these and previous BDSSCB designs, are obsolete. However, ARL recently identified and evaluated depletion mode SiC JFETs produced by United Silicon Carbide Inc. (USCi) as a replacement. Based on results from a small set of preliminary USCi packaged sample JFETs, their characteristics compare favorably to those of the SemiSouth JFETs.

## 6. References

1. Urciuoli, D. Bidirectional *Silicon Carbide Solid-State Circuit Breaker Development*; ARL-TR-6120; U.S. Army Research Laboratory: Adelphi, MD, September 2012.

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## Appendix. Datasheets for the BDSSCB v3.1 and BDSSCB v3.2 Prototypes

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# BDSSCB v3.1

600-V Bidirectional Solid-state Circuit Breaker

## General Description

This bidirectional solid-state circuit breaker (BDSSCB) module uses two SemiSouth SJDP120R085 normally-on 1200-V SiC JFETs in a common-source configuration. When triggered to the bidirectional blocking state, the module latches. The BDSSCB has an isolated gate driver providing both internal (self) and external triggering capability. The driver has a reset line to return the BDSSCB to its default bidirectional conducting state. An array of transient voltage suppression diodes is used to clamp device voltage at turn-off.



## Absolute Maximum Ratings $T_A$ = 25°C

| Symbol | Parameter | Value | Units |
|---|---|---|---|
| $V_{D-D}$ | Drain-drain voltage | 800 | V |
| $V_S$ | Supply voltage | 36 | V |
| $V_T$ | External trigger voltage | 15 | V |
| $I_D$ | Continuous drain current (note 1) | 8 | A |
| $I_{DP}$ | Pulsed drain current (note 2) | 40 | A |
| $V_{ISO}$ | Ctrl/Trg/Rst to power terminals isolation voltage | 1500 | V |
| $T_C$ | Base plate operating temperature | 100 | °C |
| $T_{STG}$ | Module storage/ambient operating temperature | 0 to 80 | °C |

1. Module baseplate should be mounted to heatsink and should not exceed $T_C$
2. Pulse width should not exceed 1 ms

## Electrical Characteristics $T_A$ = 25°C

| Symbol | Parameter | Typical | Units |
|---|---|---|---|
| $I_{DT}$ | Turn-off drain current (DC) | 4.8 | A |
| $V_{DT}$ | Turn-off voltage drop (DC) | 1.1 | V |
| $I_{DL}$ | Blocking drain-drain leakage current ($V_{D-D}$ = 800 V) | < 5 | µA |
| $T_R$ | Reset pulse duration | 6.5 to 7.5 | ms |
| $I_T$ | External trigger input current ($V_T$ = 5 V) | 3.4 | mA |
| $T_{ET}$ | External trigger delay time (≥1 µs pulse width) | 500 | ns |
| $T_{ST}$ | Self trigger delay time: ($I_D$ = 20 A)<br>(blocking $V_{D-D}$ = 600 V) ($I_D$ = 25 A)<br>($I_D$ = 30 A)<br>($I_D$ = 35 A) | 13<br>9<br>6<br>4 | µs |

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# BDSSCB v3.2

600-V Bidirectional Solid-state Circuit Breaker

This bidirectional solid-state circuit breaker (BDSSCB) module uses two SemiSouth SJDP120R045 normally-on 1200-V SiC JFETs in a common-source configuration. When triggered to the bidirectional blocking state, the module latches. The BDSSCB has an isolated gate driver providing both internal (self) and external triggering capability. The driver has a reset line to return the BDSSCB to its default bidirectional conducting state. An array of transient voltage suppression diodes is used to clamp device voltage at turn-off.

## Absolute Maximum Ratings $T_A$ = 25°C

| Symbol | Parameter | Value | Units |
|---|---|---|---|
| $V_{D-D}$ | Drain-drain voltage | 800 | V |
| $I_D$ | Continuous drain current (1) | 20 | A |
| $I_{DP}$ | Pulsed drain current (2) | 80 | A |
| $V_S$ | Supply voltage | 36 | V |
| $V_{T/R}$ | External trigger/reset voltage | 13 | V |
| $T_R$ | Reset pulse duration | 200 | µs |
| $V_{ISO}$ | Control/supply to power terminal isolation voltage | 1500 | V |
| $T_C$ | Base plate operating temperature | 80 | °C |
| $T_{STG}$ | Module storage/ambient operating temperature | 0 to 80 | °C |

1. Module baseplate should be mounted to heatsink and should not exceed $T_C$
2. Pulse width should not exceed 1 ms

## Electrical Characteristics $T_{CASE}$ = 25°C

| Symbol | Parameter | Typical | Units |
|---|---|---|---|
| $I_{DT}$ | Turn-off drain current (DC) | 9.6 | A |
| $V_{DT}$ | Turn-off voltage drop (DC) | 1.4 | V |
| $I_{DL}$ | Blocking drain-drain leakage current ($V_{D-D}$ = 800 V) | < 10 | µA |
| $T_R$ | Reset pulse duration | 50 to 200 | µs |
| $I_{T/R}$ | External trigger/reset input current ($V_{T/R}$ = 5 V) | 3.4 | mA |
| $T_{ET}$ | External trigger delay time (≥1 µs pulse width) | 1 | µs |
| $T_{ST}$ | Self trigger delay time: ($I_D$ = 20 A)<br>(blocking $V_{D-D}$ = 600 V) ($I_D$ = 25 A)<br>($I_D$ = 30 A) | 3.1<br>2.2<br>1.9 | µs |

## List of Symbols, Abbreviations, and Acronyms

| | |
|---|---|
| ARL | U.S. Army Research Laboratory |
| BDSSCB | bidirectional solid-state circuit breaker |
| IGBT | insulated gate bipolar transistor |
| JFET | junction field-effect transistor |
| SiC | silicon carbide |
| TRL | technical readiness level |
| USCi | United Silicon Carbide Inc. |

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